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09/471,244	12/23/1999	MAGED E. BESHAI	88-882836US	7184

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EXAMINER	
HAMILTON, MONPLAISIR G	

ART UNIT	PAPER NUMBER
2172	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/471,244	Applicant(s) BESHAI, MAGED E.
	Examiner Monplaisir G Hamilton	Art Unit 2172

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *6-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 13-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-30 are pending.

Election/Restrictions

2. Applicant's election of Group 1, Claims 1-5 and 13-30, in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Information Disclosure Statement

3. The information disclosure statement (IDS) is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1-5 are objected to because of the following informalities: "whose lengths are less than a predetermined value less than the length of the address" is unclear. Examiner has interpreted this to mean that the predetermine value is less that the length of the address and the prefix lengths are less than the predetermined value. This limitation needs to be clarified.

Claims 13 is objected to because of the following informalities: incorrect semi-colon usage, "steps of;" should be "steps of:". Appropriate correction is required.

Claims 18 is objected to because of the following informalities: "x, y" are undefined. Appropriate correction is required.

Claims 25 is objected to because of the following informalities: "H, K, x, y " are undefined. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052683 issued to Irwin, herein referred to as Irwin in view of US 6307855 issued to Hariguchi, herein referred to as Hariguchi.

Referring to Claim 1:

Irwin discloses a method of translating addresses of a predetermined length, comprising steps of resolving the address to a prefix, if the address is found in a primary translation table (col 2, lines 35-40), the primary translation table containing prefixes whose lengths are less than a predetermined value less than the length of the address (col 2, lines 35-40) and locations of branch data structures a plurality of secondary search units (col 2, 38-44; col 7, lines 17-25); performing a secondary search in the secondary search units (col 9, lines 30-45), if the primary translation table indicates the locations of branch data structures to begin each secondary search for prefixes whose lengths are larger than the predetermined value (col 8, lines 1-15; col 8, lines 15-25) and translating the addresses to prefixes, if the prefixes are found in the secondary search (col 5, lines 60-65; col 5, lines 64-66; col 9, lines 30-42).

Irwin does not explicitly disclose, "performing a secondary search in the secondary search units in parallel".

Hariguchi discloses performing a secondary search in the CAM (secondary search) units in parallel (col 5, lines 50-55; col 6, lines 5-15).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Irwin such that the secondary search is performed in parallel. One of ordinary skill in the art would have been motivated to do this because it would allow the system perform faster translations (Hariguchi: col 5, lines 50-55).

Referring to Claim 28:

Irwin discloses an address translation apparatus for telecommunications networks in which packets are transported to addresses contained therein, comprising: an address separation unit for separating from a packet an address to be translated (col 6, lines 38-45); primary translation unit having a primary translation table for translating the address to a prefix (col 8, lines 10-15), the primary translation table containing prefixes whose widths are less than a predetermined value (col 2, lines 35-40) and locations of branch search data structures in a secondary search units (col 2, 38-44; col 7, lines 17-25); and a plurality of secondary search units for performing secondary searches, each secondary unit having the branch search data structure for performing each secondary search (col 8, lines 1-15; col 8, lines 15-25; col 9, lines 33-43) and translating the address to a prefix, if the primary translation table indicates the location of a branch search data structure to begin the secondary search (col 5, lines 60-65; col 5, lines 64-66; col 9, lines 30-42).

Irwin does not explicitly disclose, "performing a secondary search in the secondary search units in parallel".

Hariguchi discloses performing a secondary search in the CAM (secondary search) units in parallel (col 5, lines 50-55; col 6, lines 5-15).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Irwin such that the secondary search is performed in parallel. One of ordinary skill in the art would have been motivated to do this because it would allow the system perform faster translations (Hariguchi: col 5, lines 50-55).

Referring to Claim 2:

Irwin in view of Hariguchi discloses the limitations as discussed in Claim 1 above. Irwin further discloses selecting one of a plurality of secondary search units in response to the location of a branch data structure (col 8, lines 10-35).

Referring to Claim 3:

Irwin in view of Hariguchi discloses the limitations as discussed in Claim 2 above. Hariguchi further discloses buffering addresses to be translated at the secondary search units for secondary searches so that a plurality of addresses are translated in parallel in an orderly fashion (col 13, lines 25-30).

7. Claims 4 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052683 issued to Irwin, herein referred to as Irwin in view of US 6307855 issued to Hariguchi, herein referred to as Hariguchi further in view of US 6563823 issued to Przygienda, herein referred to as Przygienda

Referring to Claims 4 and 29:

Irwin in view of Hariguchi discloses the limitations of Claims 3 and 28 above.

Irwin in view of Hariguchi does not explicitly "scrambling the address according to a predetermined reproducible formula".

Przygienda discloses scrambling the address according to a predetermined reproducible formula (col 7, lines 45-60).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Irwin in view of Hariguchi to scramble the address. One of ordinary skill in the art would have been motivated to do this because it would provide a way of building/organizing the routing table (col 7, lines 20-25).

Referring to Claim 30:

Irwin in view of Hariguchi in view of Przygienda discloses the limitations as discussed in Claim 29 above. Irwin further discloses a selector for selecting a secondary search unit for performing the secondary search (col 8, lines 17-30, 55-65).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052683 issued to Irwin, herein referred to as Irwin in view of US 6307855 issued to Hariguchi, herein referred to as Hariguchi further in view of US 5909440 issued to Ferguson, herein referred to as Ferguson.

Referring to Claim 5:

Irwin in view of Hariguchi discloses the limitation as discussed in Claim 2 above.

Irwin in view of Hariguchi does not explicitly disclose, "selection of the secondary search units is performed according a round-robin discipline".

Ferguson discloses selection of the secondary search units is performed according a round-robin discipline (col 5, lines 40-45).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Liao such that the plurality of second search engines are chosen based on a round-robin scheduling discipline. One of ordinary skill in the art would have been motivated to do this because it would speed up route processing (Ferguson: col 5, line 42-44).

9. Claims 13-19 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052683 issued to Irwin, herein referred to as Irwin in view of US 6526055 issued to Perlman herein referred to as Perlman

Referring to Claims 13:

Irwin discloses a method of resolving B bit long addresses of packets into prefixes of any length up to B by the use of a data structure which comprises a length sorted table Q (col 2, lines 35-40; col 13, lines 45-65; Lookup table) and a plurality of secondary search units (col 12, lines 54-56; CAM Table), table Q containing data related to prefixes of length less than A, A<B comprising steps of (col 13, lines 14-18, 44-48); (1) indexing table Q by using the first A bits of an address to generate a corresponding prefix of length equal to or less than A, or a pointer to a secondary search unit (col 13, lines 45-65; Lookup Table).

Irwin does not explicitly disclose "each secondary search units including tables V and T which are in one-to-one correspondence to one another and each consists of a 2xM memory, M being a positive integer (2) accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order; (3) accessing table T of the secondary search unit at each successive location corresponding to the location of table V accessed in step (2); and (4) reading a valid data contained at the location in table T, the valid data being a prefix of length more than A"

Perlman discloses each secondary search units including tables V and T which are in one-to-one correspondence to one another and each consists of a 2xM memory, M being a positive integer (col 14, lines10-20; Fig. 6c; col 11, lines 20-25) (2) accessing table V of the

secondary search unit indicated by the pointer using each successive remaining bit of the address in order (col 12, lines 5-15); (3) accessing table T of the secondary search unit at each successive location corresponding to the location of table V accessed in step (col 14, lines 40-55) (2); and (4) reading a valid data contained at the location in table T, the valid data being a prefix of length more than A (col 12, lines 15-20).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teaching of Irwin to include a memory storing two tables for each search unit. One of ordinary skill in the art would have been motivated to do this because it would increase the speed for determining the correct output port (Perlman: col 14, lines 53-56).

Referring to Claim 14:

Irwin in view of Perlman discloses the limitations of Claim 13 above. Perlman further discloses steps (2)-(4) are performed in one or more of the secondary search units in parallel (col 14, lines 10-20).

Referring to Claim 15:

Irwin in view of Perlman discloses the limitations of Claim 14 above. Irwin further discloses each secondary unit comprises one or more search branches and a pointer to a secondary search unit indicates the identity of the secondary unit and a branch number h (col 9, lines 35-40, 59-65);

Irwin does not explicitly disclose "data relating to two or more search branches are interleaved in tables V and T of a secondary unit, the method further comprises a step of

accessing table V at a location indicated by the branch number h of the secondary unit identified by the pointer."

Perlman discloses data relating to two or more search branches are interleaved in tables V and T of a secondary unit (Fig. 6c; col 20-25), the method further comprises a step of accessing table V at a location indicated by the branch number h of the secondary unit identified by the pointer (col 14, lines 40-55).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teaching of Irwin to include a memory storing two interleaving tables for each search unit. One of ordinary skill in the art would have been motivated to do this because it would increase the speed for determining the correct output port (Perlman: col 14, lines 53-56).

Referring to Claim 16:

Irwin in view of Perlman discloses the limitations of Claim 15 above. Perlman further discloses the step of accessing table V in each identified secondary search unit comprises further steps of: (5) accessing table V by using the first bit of the remaining bits of the address at a location identified by branch number h (col 12, lines 5-25); (6) reading table V at the location which indicates a next location of table V (col 12, lines 15-20); (7) continue accessing and reading each successive location using each successive bit of the remaining bits until the Bth bit (col 15, lines 19-25); and continue reading the valid data contained at the location in table T corresponding to the successive locations read in the step (7) (col 14, lines 40-55).

Referring to Claim 17:

Irwin in view of Perlman discloses the limitations of Claim 16 above. Perlman further discloses accessing table T at a location corresponding to each successive location accessed in steps (5)-(7) recording the data contained at each accessed location of table T; and reading the valid data contained at the latest previously accessed location if the last accessed locations contained no valid data (col 14, lines 40-55).

Referring to Claim 18:

Irwin in view of Perlman discloses the limitations of Claim 16 above. Perlman further discloses, wherein u_j is the j^{th} bit of the B-bit received address, and the address is known to belong to branch h, the steps of accessing and reading table V and T in each secondary search unit are performed as follows to generate a prefix t:

y=h, t=0,

for $1 \leq d \leq B$

{

x=u_d;

if (T(x, y)>0) t=T(x, y));

y=V(x, y)

if V(x, y)>0, y= V(x, y)

} (col 12, lines 5-25; col 14, lines 40-55).

Referring to Claim 19:

Irwin in view of Perlman discloses the limitations of Claim 16 above. Perlman further discloses the step of reading the valid data contained at the location in table T is replaced by steps of: reading an indicator contained at the location in table T; accessing a storage device at a location indicated by the indicator; and reading the valid data contained at the location in the storage device (col 14, lines 40-55).

Referring to Claim 22:

Irwin in view of Perlman discloses the limitations of Claim 13 above. Irwin further discloses length sorted table Q provides an indication of `00' if the address cannot be resolved, "01" if the prefix is found (col 11, lines 50-55), and" 10", if a further search is required in a respective secondary search unit in that a "10" outcome is associated with a branch number (col 34-43).

Referring to Claim 23:

Irwin discloses an apparatus for address translation of a packet, comprising: a parsing block for receiving the packet and parsing address, each address having length B, B being a positive integer (col 2, lines 35-40; col 13, lines 45-65); an indexing block for selecting the first A binary bits of each received address, A being a predetermined positive integer and A<B and for directly accessing a sorted prefix directory by the first A binary bits, the sorted prefix directory containing translated prefixes of length N equal to or shorter than A and data

specifying one of a plurality of secondary search units (col 6, lines 38-55; col 13, lines 14-18, 44-48);

Irwin does not explicitly disclose "the plurality of secondary search units having the plurality of secondary memories for searching in parallel through the secondary memories specified by the indexing block for prefixes of length N longer than A, each secondary memory comprising tables V and T in that tables V and 'T are in a one-to-one 5 correspondence to one another and each consists of a 2xM memory. M being a positive integer, table V for accessing successive location for each successive bits above A of the addresses and table T for translated prefixes at a location corresponding to the location accessed in table V."

Perlman discloses the plurality of secondary search units having the plurality of secondary memories for searching in parallel through the secondary memories specified by the indexing block for prefixes of length N longer than A (col 12, lines 5-20), each secondary memory comprising tables V and T in that tables V and 'T are in a one-to-one correspondence to one another and each consists of a 2xM memory (col 14, lines 40-55), M being a positive integer(col 14, lines 40-55), table V for accessing successive location for each successive bits above A of the addresses and table T for translated prefixes at a location corresponding to the location accessed in table V (col 11, lines 20-30; col 14, lines 10-20; col 12, line 55-col 13, line 5).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teaching of Irwin to include a memory storing two tables for each search unit. One of ordinary skill in the art would have been motivated to do this because it would increase the speed for determining the correct output port (Perlman: col 14, lines 53-56).

Referring to Claim 24:

Irwin in view of Perlman discloses the limitations of Claim 23 above. Perlman further discloses each prefix of length longer than A belong to any of prefix trees and each secondary memory containing prefixes of one or more prefix tree (col 12, lines 5-20; col 16, lines15-25).

Referring to Claim 25:

Irwin in view of Perlman discloses the limitations of Claim 23 above. Perlman further wherein tables V and T of each secondary memory have data structures containing translated addresses J for addresses belonging to address tree branch h and 1 <_h<_H, K=H+F, y=h+F, F being an arbitrary integer offset representing a reference memory address in that J is generated as follows:

for $1 \leq j \leq M$

{

for $1 \leq d \leq m_j$

{ $x = D_{j,d}$

if $V(x, y) > 0$, $y = V(x, y)$

else {K-->K+1, $V(x, y) = K$. $y=K_j$ }}

for $d = m_j$, $x = D_{j,d}$, $T(x, y) = J$

}

wherein a plurality of addresses are sorted in a sorted address directory R, the j^{th} address in position j in directory R has m_j bits; the bit in position d, $0<d<m_j$, in the j^{th} index, is denoted $D_{j,d}$ and the value of $D_{j,d}$, is either "0" or "1" (col 12, lines 5-25; col 14, lines 40-55).

10. Claims 20-21and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052683 issued to Irwin, herein referred to as Irwin in view of US 6526055 issued to Perlman herein referred to as Perlman further in view of US 6563823 issued to Przygienda, herein referred to as Przygienda

Referring to Claims 20 and 26:

Irwin in view of Perlman discloses the limitations of Claim 19 and 25 above.

Irwin in view of Perlman does not explicitly "scrambling all the bits of the addresses to be translated according to a reproducible formula".

Przygienda discloses scrambling the address according to a predetermined reproducible formula (col 7, lines 45-60).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Irwin to scramble the address. One of ordinary skill in the art would have been motivated to do this because it would provide a way of building/organizing the routing table (col 7, lines 20-25).

Referring to Claims 21 and 27:

Irwin and Perlman in view of Przygienda disclose the limitations of Claims 20 and 26 above. Przygienda further discloses the reproducible formula is a bit reversal of all the bits in the addresses (col 7, lines 20-25).

Prior Art

11. US 6430527 issued to Waters, Gregory M. et al. Waters discloses prefix searches for directing internet data packets are performed in a prefix search integrated circuit. The integrated circuit includes an array of search engines, each of which accesses a prefix search tree data structure to process a prefix search. An SDRAM is dedicated to each search engine, and SDRAMs share address and control pins to plural search engines on the IC chip. Internal nodes of the tree data structure are duplicated across banks of the SDRAMs to increase bandwidth, and leaf nodes are stored across the SDRAM banks to reduce storage requirements. Within each search engine, data stored in a data register from an SDRAM is compared to a prefix search key stored in a key register. Based on that comparison, an address is calculated to access further tree structure data from the SDRAM. Packet descriptors containing search keys are forwarded to the search engines from an input queue and the search results are forwarded to an output queue, the same packet order being maintained in the two queues.

US 6421342 issued to Schwartz, Steven J. et al. Schwartz discloses an apparatus and method for forwarding packets of data across a switching node on a network are disclosed. A packet of data to be forwarded includes a destination address, which can be partitioned into a plurality of subaddress fields. To improve speed of packet forwarding, destination addresses are processed in a pipelined fashion. To that end, the system includes a plurality of pipelined subaddress processors which process a respective plurality of subaddress fields of the destination addresses. Addresses are received during addressing intervals. During a first

interval, a first subaddress of a first packet is processed by a first subaddress processor. During a next interval, a second subaddress processor processes a second subaddress field of the first packet destination address while the first subaddress processor processes the first subaddress field of a destination address of a next packet. Each destination address is stored in a table which associates destination addresses with output paths out of the switching node. The table is partitioned into portions associated with the subaddress fields. Each subaddress processor accesses the portion of the table associated with its subaddress to route the packet out of the node along the correct output path to facilitate delivery of the packet at the destination node.

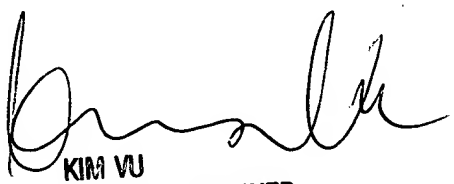
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monplaisir G Hamilton whose telephone number is 1703-305-5116. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on 1703-305-4393. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 1703-305-3900.

Monplaisir Hamilton



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